UCRL-MI-201013

# A CMOS Based LSST Imaging Conceptual Design for Enhanced Dynamic Range

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## *Abstract*

A conceptual design for an LSST imaging system is presented which employs a multiple capture per image scheme originally developed to enhance dynamic range in video applications.

## *Intro to LSST imager*

The LSST imager system is unique in size and data rate. With ~2.5 billion 16+ bit pixel values being generated every ~15 seconds, system components must have capabilities well beyond those in common use today. Even with an 8+ year timescale to operations, the definition and design of the imaging system must be firm within as little as two years. The LSST investigators must evaluate the competing possibilities and generate a baseline design during this first phase.

The critical detector requirements assuming 10 second exposures are:

1.) 8-10 micron pixel size
2.) >95% fill factor
3.) high QE (>.6@400nm, >.85@600-900nm, >.45@1000nm)
4.) full well > 90000 electrons
5.) read noise < 5 electrons
6.) readout time < 2 seconds.

No such detectors are readily available. State-of-art and under-development technologies include: thick high-resistivity silicon back-illuminated CCDs and hybrid silicon photodiode-CMOS array detectors. This document is principally concerned with addressing items 4, 5, and 6 above, that is, dynamic range, signal-to-noise, and readout time.

There are problems with CCDs. The need for a mechanical shutter, high power dissipation, and a dwindling manufacturer base, have generated a growing interest in CMOS based detectors. However, existing CMOS solutions are not yet capable of meeting the requirements either.

Much of the discussion of CMOS based detectors for LSST has centered on commercially developed imagers (Raytheon, Rockwell) that have evolved from hybrid multiplexer arrays developed for infrared imaging. The principal development hurdle is to scale down hybrid bonding techniques to the 8-10 micron pixel pitch needed by LSST or to find alternate techniques. The nominal mode of operation under discussion for LSST is a sequence of two exposures at ~10 seconds, each followed by a ~2 second readout and a telescope re-pointing of ~5 seconds (overlapped

with the second readout). Analog data for each pixel would then be digitized at 16 bits resolution. The sequence would then be repeated as the telescope marches through its set of fields covering the visible sky once every few nights. The operation is essentially the same as if traditional CCDs were used and of course was spelled out with a CCD based focal plane as the default position.

## *Why stop there?*

Academic and commercial research in CMOS imaging has demonstrated capabilities that can be exploited. In particular, it is highly desirable to achieve extended dynamic range and enhanced signal-to-noise ratios. A major benefit for photometric and astrometric calibration can be achieved by maintaining sensitivity to faint objects while simultaneously allowing bright objects (eg. ~12 Mag) to be imaged. These objectives, and additional flexibility in cosmic ray rejection and transient detection, may be implemented by using the non-destructive readout, pixel addressability and multiple capture functions that have been developed for CMOS based imagers.

To flesh out the possibility of applying these ideas, a conceptual design is presented below in a brief format. An expanded discussion of the various design components and questions to answer then follows.

## *A conceptual design*

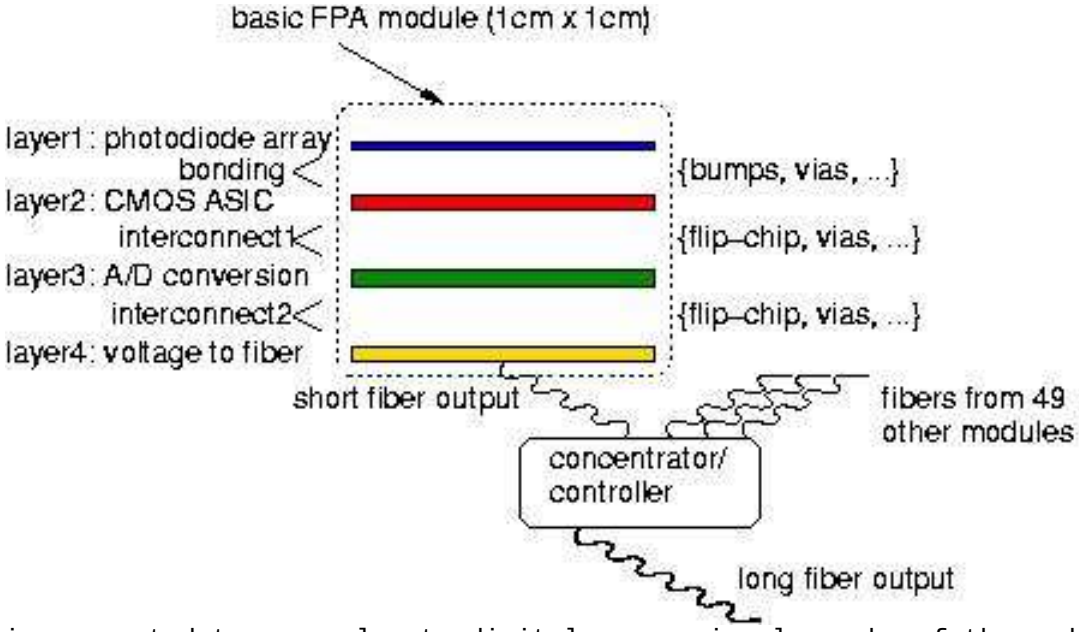
This design is a radical departure from standard CCD style readout as it capitalizes on CMOS imager development that has been carried out in the academic and commercial arenas. The motivation for the method described below is to extend the dynamic range of the images obtained for both bright and faint regions relative to the default, CCD-like, operation. The concept is to readout the focal plane every 50 milliseconds using 12 bits of digitization. Each non-destructive readout takes place in 1 millisecond and is followed by a 49 millisecond integration period. Individual pixels are reset as needed after readout. Each “exposure” for the LSST archive would be constructed by optimally combining ~256 samples taken over a 12.8 second period. Naively, the dynamic range is expanded by ~256[1] in bright regions (because of pixel resets). Faint regions also benefit from the multiple sampling, which yields lower effective read-noise. Further details of the focal plane modules, functionality, and data flow are described below.

The LSST focal plane will consist of ~2500 imager modules, each consisting of a ~1cm x 1cm array of 1024 10 micron pixels. The imager modules convert the integrated flux of incoming photons to digitized signals. The signals are routed from the module via a short optical fiber link to a concentrator module. The imager modules are grouped in sets of 50, with one concentrator module for each set. The concentrator modules serve two functions. They control the operation of the sensor modules and route the digitized signals from the camera

[1] 256 times the 12-bit maximum of 4096 – value in electrons depends on the gain – see below.

housing to data acquisition modules external to the telescope. The external modules serve the function of assembling the 50 multiplexed imager data streams containing the 2500 sub-images for injection into the image processing pipeline.

Each imager module comprises 4 layers (figure 1): a photo-diode array, bonded to a CMOS active pixel matrix, followed by an analog-to-digital conversion layer and an optical fiber output layer. For this discussion it is assumed that the bonding "problem" between the photo-diode array and the CMOS ASIC is solved. The CMOS pixels are active photogate style optimized for low read noise with non-destructive readout and individual reset functionality. The pixel array is divided into 32 sets of 32 columns with a total of 32 outputs. The pixel array layer




is connected to an analog-to-digital conversion layer by of the order of 100 connections using standard flip-chip methods. The ADC layer, with 32 12-bit converters, also contains additional circuits for timing, resetting, and routing. Using a similar approach, of the order of 50 data/control connections will route data from the ADCs to the optical transmission layer.

**Figure 1. Basic schematic for imager modules**

Photometric accuracy (of the detector) must be better than 1 part in 1000. Hence pixel signals must be measured with >10 bit accuracy and digitization will be carried out at 12 bits of resolution with a nominal gain of ~3 electrons/adu. For additional flexibility, the digitized data will be transferred at 16 bits. The design relies on a row-based readout (figure 2). Each 1024 pixel row is read out via 32 outputs at ~30 ns per pixel (33 MHz) for a total of ~1us per row. It will take 1ms to digitize and readout the entire 1024x1024 sensor. The thirty-two ADCs will operate in parallel. Each digitization includes a mechanism for resetting of the pixel well if the pixel is likely to saturate before the next digitization. If a pixel is reset, the unused $13^{th}$ bit will be set to flag the event. In addition it may be possible and advantageous to have a dual gain system, where pixels above ~12000

electrons are digitized at ~24 electrons/adu to allow for up to ~100000 electrons digital- full-well to fit in the 4096 adu limit of the 12 bit ADC converter. Again, an additional flag (14th bit) would be used to indicate the gain setting. Every 30ns a 32 x 16-bit word will be transferred over a 16Gbit/s short optical link to the concentrator. With 12 bits representing the pixel signal, the remaining 4 bits will be used as flags for pixel reset, pixel gain, and possibly other quantities. The sensor readout sequence would take place every 50 ms and require powering-up of the ADCs and optical fiber circuits for just ~1.5 ms yielding a ~3% duty cycle. That is, the imager modules would be fully read out at 20 Hz with digitization to 12 bits, pixel reset based on signal level, and possibly a dual-gain approach. Based on existing 12 bit ADC converters operating at 33 MHz, each module would consume ~300 milli-watts. This figure may be reduced as lower power ADC converters come on the market.

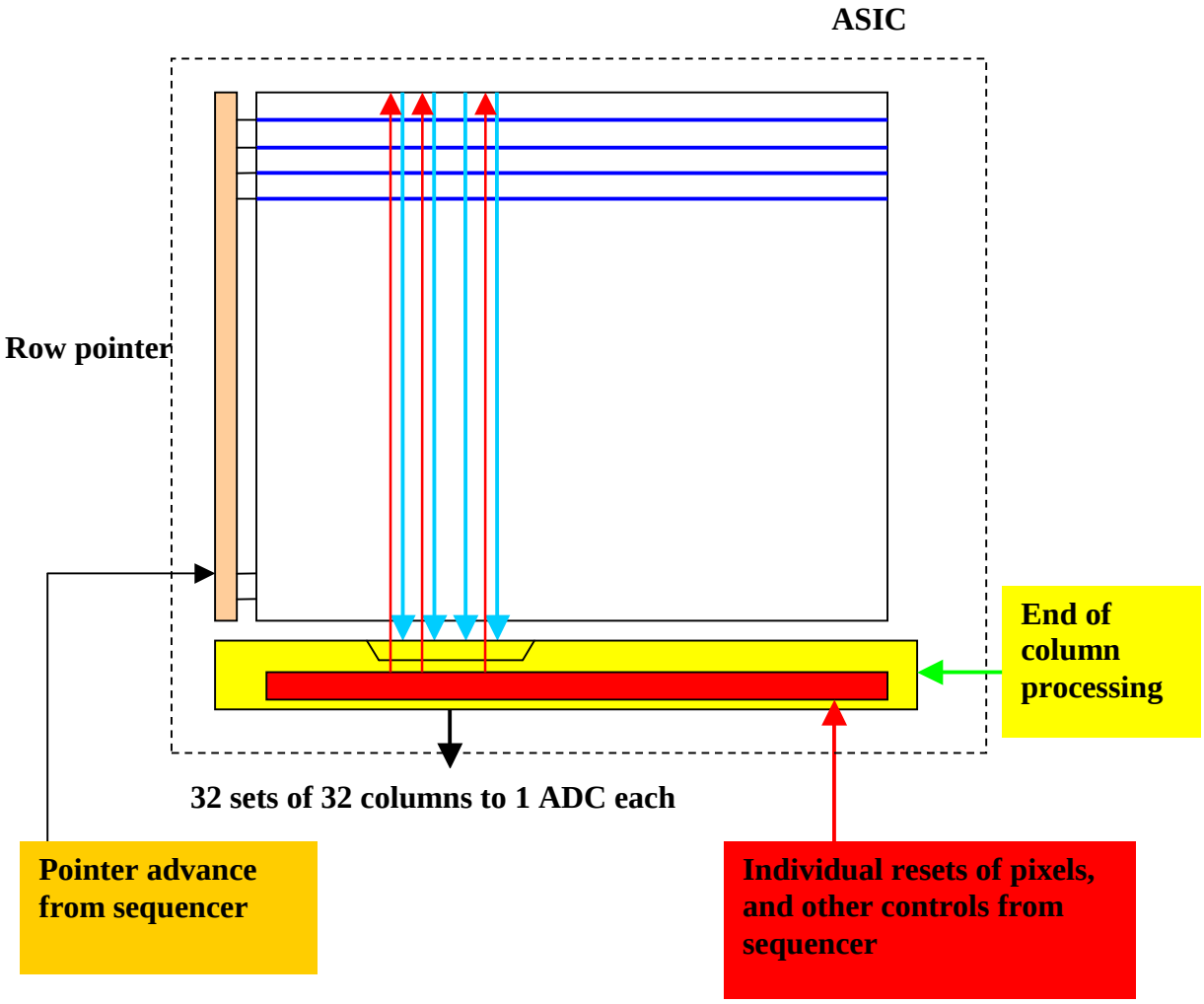


**Figure 2** Analog processing ASIC for a 1Kx1K pixel array. All columns are read out in parallel. A row pointer controlled by the sequencer defines which pixel on each column is to be read. Signals (red) generated by the sequencer define which pixels are to be reset. Assuming a pixel size of 10μmx10μm, overhead of a pixel on the vertical sides and on the top side of the 1cm x 1cm array of 10μm, and a 50μm overhead on the bottom side the effective area is about 99% of the total area.

Each concentrator module would accept 50 incoming fibers and output a single fiber to a control room facility where the pixel images would be built up from the multiple capture streams. It would sequentially trigger the readout of the 50 imager modules at 1 per milli-second. The output fiber would then operate at ~100% duty cycle. Each concentrator module is estimated to consume less than 1 watt. The net power consumption for the entire imager array and concentrator modules is under 1000 watts and includes all imaging functions inside the Dewar.

For ~2500 1kx1k modules, grouped by 50, with one concentrator module per group, there will be 50 fibers running at ~100% duty cycle with a data rate of ~16 Gbit/sec feeding a cluster of data acquisition "computers". These will combine the incoming 20 Hz data stream to build integrated images with effective exposure times of ~10-20 seconds. With 50 groups of 50 1kx1k modules, running at 20 Hz, a single module in each group would readout during each 1ms readout period. The multiplexing scheme is:

```
2500 x 1024 ---> 2500 x 32 ---> 2500 x 1 ---> 50
 pixel-row     ADC channels    short-fiber  long-fibers.
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Moving the task of combining the multi-sample data stream physically away from the camera/telescope structure allows for optimization, flexibility, and the use of cheaper hardware to carry out the task. Each imager module (1kx1k) will produce 2Mbytes/readout or 512 Mbytes per nominal 256 cycle image acquisition. There will be a set of 2500 "processes" (>1 per cpu perhaps) which would optimally combine the data stream into a single ~16-18 bit/pixel image which includes cosmic ray rejection and expanded dynamic range.

## *Discussion*

### Multiple Capture Scheme

The design rests on using multiple non-destructive reads with signal level triggered resets to measure the photon flux received by each pixel. The CMOS architecture provides the possibility of non-destructive reads, addressable pixel reset, and shutterless operation which are required for this scheme. In more detail, consider the set of pixel values, $\{Q_j\}$ (j=1,…,256), which must be combined to form a single LSST image. An initial sample, $Q_0$, is taken after a global reset of all pixels at time t=0. The initial sample contains readout noise, reset noise, and offset fixed pattern noise. In the case of no resets, subsequent reads have a value $Q_j = (i_{ph} + i_{dc})j\tau$ + (noise-terms), where $i_{ph}$ is the photocurrent, $i_{dc}$ is the dark current, $\tau$ is the 50 millisecond

sample time, and the noise-terms include readout noise, reset noise, offset fixed pattern noise and shot noise. When $i_{ph}$ is large enough to cause resetting of the pixel well, the expression becomes:

$$Q_j = (i_{ph} + i_{dc})(j-j_m)\tau + (\text{noise-terms}),$$

Where $j_m$ is the index of the $m^{th}$ reset and additional noise terms are added for each reset. The resulting set of values, $\{Q_j\}$, must then be used to estimate the quantity: $(i_{ph} + i_{dc})$. On the bright end, the pixel value will have been reset many times, while on the faint end, only the late samples will have a signal usefully above the noise level. Work on determining an optimal algorithm for combining the samples has already been well developed (Liu 2002, Fowler 2002) albeit without the dual gain. Methods for combining the full set, and recursive real-time methods have been analyzed. The upshot is that these methods are straightforward and can yield greatly increased dynamic range at the bright end via the multiple resets and at the faint end by optimally weighting the multiple samples. In particular, the last samples are heavily weighted in the faint pixel case and the read noise is reduced as a function (~sqrt()) of the number of useful (high weight) samples. These methods were developed for the 1000 samples/sec 8-bit regime but should apply equally well to the 20 samples/sec 12-bit regime described here. Either during the multi-capture image construction, or after, the usual astronomical image calibration techniques would also be applied. In particular, dark subtraction and flat field corrections would be applied. This technique has several other benefits. The nominal read noise requirement for LSST (5 electrons) constrains the CMOS technology process features at or above 0.25 microns. The multiple capture scheme may allow relaxation of the read noise requirement for a single read which may make device fabrication easier. Also, cosmic rays could easily be rejected from the data stream, making a second “observation” unnecessary. In particular, the nominal 2 exposure {10s exposure, 2s readout, 10s exposure, slew&readout} scheme would be replaced by a single “image” {256 samples in 12.8 seconds, slew&combine image stream} thereby increasing the area coverage rate of the survey. A more complete analysis and modeling campaign of noise and dynamic range is needed for the 20 Hz multiple capture scheme described above, however the work that has been carried out and published (Liu, Fowler and others) shows that the approach is worth pursuing.

## CDS and multiple capture

Correlated Double Sampling (CDS) circuitry will be located on each set of 32 columns at the multiplexer output before presentation of the signal amplitude to the ADC. It will remove the fraction of the noise and other effects (i.e. biases drift) that affect the response of the pixels as long as they remain constant between the two sampling pulses (the component of noise and other effects at frequencies substantially below the interval between the sampling pulses). Different implementations are possible depending on the frequency spectrum of the effects and noise to be removed. In the simplest case the reference/background is sampled at the start of the readout of each row and is used for each cluster of 32 columns. The distance between samples of the background by the CDS is ~1μs. A more extensive case would operate the CDS at pixel readout intervals of 30ns.

Effects such as injection levels associated with the readout are dependent on pixel level circuitry and signal strength. They constitute Fixed Pattern Noise. With the proposed multiple readout scheme these

effects can be perceived as being cumulative hence deleterious to the intent of minimizing pixel noise. It is suggested that these effects can be measured during a characterization/calibration phase of the modules. Correction data stored in look up tables is used in real time or prior to aggregating the data from the 256 readouts. It must be noted that such look up tables may require 20 to 40 points per pixel and possibly 100Gbytes of storage but this is readily achievable using currently available 1Gbit memory chips. Alternatively if these corrections are not made in real time the overall storage needed will reside on disk and is insignificant in regard to total storage needs. The topology of the pixel circuitry must ensure that reading out does not affect the charge stored under the pixel. Several recent publications including (Fowler 2002) seem to indicate that the noise can be reduced substantially using multiple readouts. It should be a priority to verify that their conclusions can be extended to the case of the focal plane of the LSST.

## Physical layer 3:ADC conversion details

With the CMOS architecture, it is possible to imagine complete parallelism with digitization implemented inside each pixel. In fact this has been carried out (Liu 2002) in the small array, 1000 frames/sec 8-bit regime. However, the LSST requirements on the accuracy favor a separation of the analog readout from the digitization function. In this conceptual design, space considerations argue for the choice of 32 ADC converters on the third physical layer rather than going to one ADC converter per column or with fewer, faster converters.

Also it must be noted that for a hybrid detector, the entire ASIC pixel area is available for readout functionality and hence it would be possible to envision further in pixel functionality with the fully parallel scheme mentioned above as an example. For this discussion however, an architectural commonality between monolithic and hybrid CMOS detectors has been maintained.

The function of the 3rd physical layer is to sequence the real time digitization including the reset of individual pixels during readout, to attach additional information such as: gain setting and pixel reset to the digitized signal and to route the pixel data to the transmission link. Under computer/operator control the sequencer operating modes and reset threshold are programmable. The building blocks of the layer are:

- The sequencer: a simple state machine that can be implemented in a FPGA or a custom CMOS ASIC.
- The ADCs: assuming 3e-/ADU, a 12-bit ADC will support maximum signals of ~12,000e-. If physical layer 2, the analog processing layer supports dual gain operation an optional 24e-/ADU with a maximum signal of ~96,000e- will be available on intense signals. The 12-bit resolution ADCs will support 32 columns each. Thirty-two ADCs operating at less than 40MHz are needed to digitize the 1Kx1K pixel module in about 1ms. Current technology provides 4 ADCs operating at up to 65MHz in a single package. Power consumption is of the order of 250mW per ADC but the active duty cycle is only ~<3%. A power down pin allows the power to be reduced to very low levels when digitization is not needed. The ADCs may be purchased as dies in order to optimize the packaging. It is

expected that future ADC offerings will provide lower operating power as well as more ADCs per die.
- Multiplexing structures to route the data to the transmission link.
The functionality of the layer is shown on figure 3.

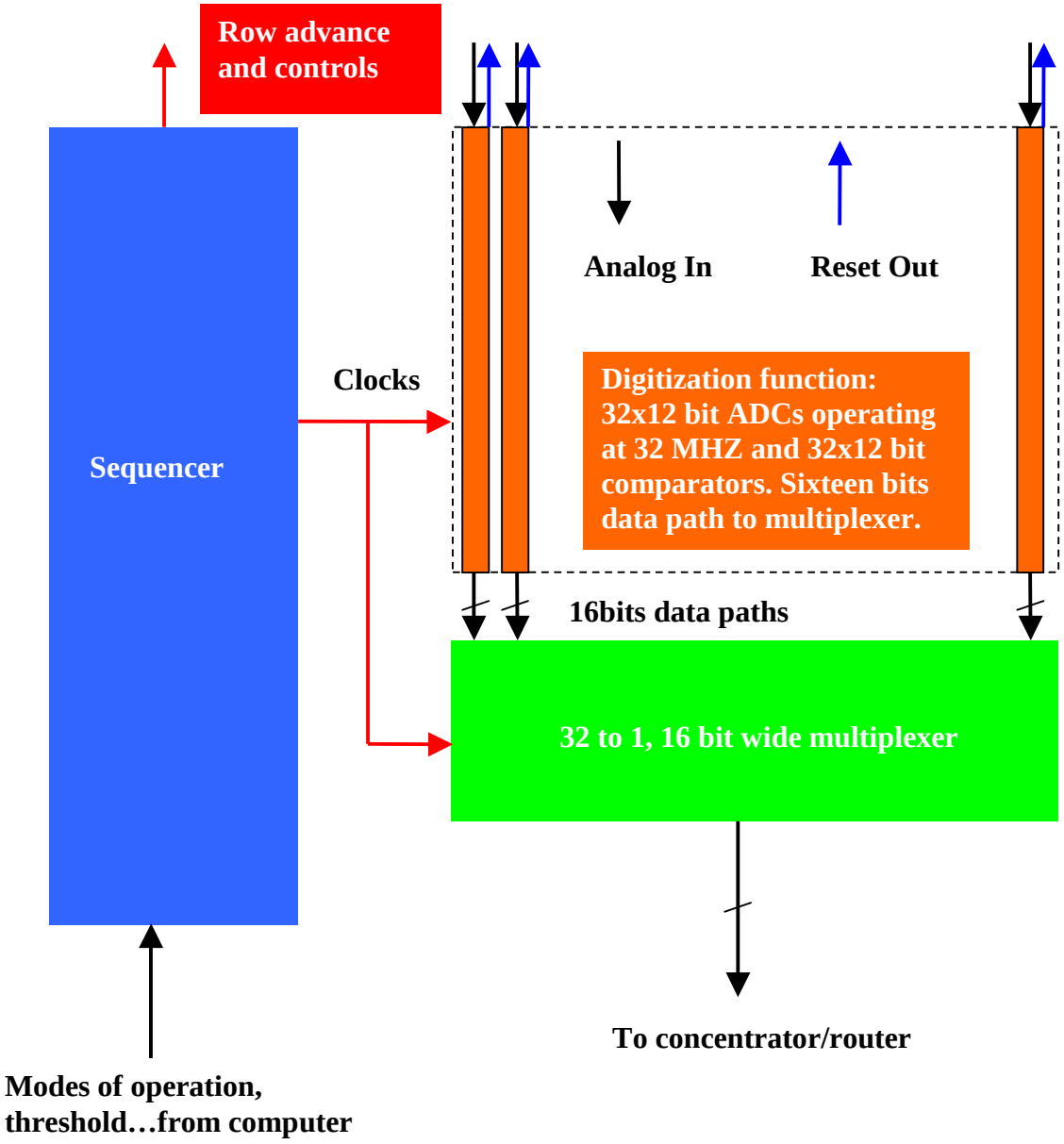


**Figure 3. Physical Layer 3**

## Power Dissipation

The design assumes a currently available off the shelf 12bit analog to digital converter. The following estimates can be made per 1Kx1K device:

| | |
|---|---|
| Sensor and analog readout: | 20mW |
| ADCs and sequencer*: | 250mW |
| Transmission link**: | 10mW |
| Total: | ~300mW |

* Assumes 1ms total readout time, ADCs being active 3% of the time (1.5ms per readout, 49ms integration). Quad ADCs consuming 940mW when active, 3 mW when powered down with 8 quads used per 1Kx1K.
** Assumes 500mW per 10Gbit short haul link operating 2% of the time.

The total power dissipation of the focal plane is 300mWx2500 or ~750W

Taking into consideration the design and technology driven reduction in power over the last 6 years of 12 bit ADCs operating at digitization rates of ~40MHz and assuming that the trend continues as driven by market demands, the power dissipation of a 1Kx1K could be reduced by a at least 1/3 over the next few years.

## Physical layer 2: Analog processing/Reset scheme

The analog processor associated to each pixel consists of a buffering structure to the column, the reset and gating structure. The readout is under the control of the sequencer part of physical layer 3. The readout is column based meaning that signals from pixels sitting on the same column will follow the same physical path to the ADC. When the sequencer selects a row all pixels on that row will feed their signal to the corresponding column analog data path. In regard to the analog readout all columns operate in parallel at a cycle per pixel (row) of the order of 1$\mu$s.

Thirty-two adjacent columns feed their signals through a multiplexer to a common ADC. In order to cover a large signal range up to ~100,000e- a dual gain mode can be implemented. The resulting dynamic range will then be of the order of $2x10^7$ covering an extended range of stellar magnitudes.

The reset of individual pixels will be decided based on their signal level in the previous recording. If a dual gain mode is implemented the decision to reset may be made by the comparator selecting the gain or by a digital comparator to be associated with each ADC. In each case a digital signal will be sent on the relevant column triggering the reset. In either case a threshold value originating with the experimenter will be provided by the sequencer. In addition a global reset will be provided that simultaneously reset all pixels. A functional sketch of the layer is given figure 2.

## *Areas for further investigation*

## Overall system definition and tradeoffs:

1. Operating modes, relations to the sequencing of the telescope.
2. System interdependencies: mechanical accuracy, power dissipation, packaging, installation, maintenance.

## Physical layer 1:

1. Expanding use of indium bumping to 10μm pitches.
2. Other bonding methods i.e.: anisotropic conductive films, SIO CMOS
3. Material deposition: what material? Si, SiGe, What type of deposition? Amorphous, epitaxial.
4. Characterization methods of physical layer 1 regardless of the technology used.

## Physical Layer 2:

1. Modeling of noise performance under the READ/RESET and READ/NO RESET scenario.
2. Prototyping a test device which can provide results that can be extrapolated to a 1Kx1K.
3. Characterization methods of physical layer 2.

## Physical layer 3

1. Characterize ADC performance at envisioned speed.
2. System design: detailed definition of functionality, optional features, implications on power dissipation and packaging.
3. Sequencer definition.

## Physical layer 4:

1. Multi-module backplane definition. Packaging and assembly related issues. Maintainability.
2. Search for a low power optical link. Commercial or specific.
3. Concentrator/Router

## *Summary*

The proposed conceptual design offers substantive advantages over the “standard” CCD or CMOS readout in regard to dynamic range, readout time, possibly signal to noise management and certainly flexibility of use. It relies fundamentally on the premise that hybrid pixels arrays at 10μm pitch are feasible whether using a flip chip approach or a deposition approach. Clearly this assumption must be verified as soon as possible. The design is also fully compatible with a monolithic approach if deemed acceptable. This conceptual design requires a steep up front investment in development but is portent of major costs reductions at design, construction, characterization and operation times.

This work was performed under the auspices of the U.S. Department of Energy, National Nuclear Security Administration by the University of California, Lawrence Livermore National Laboratory under contract No. W7405-ENG-48

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